



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,314	09/02/2003	Takehiro Sato	031098	1723
38834	7590	12/10/2004	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/652,314

Applicant(s)

SATO, TAKEHIRO

Examiner

Julio J. Maldonado

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 18 and 19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (U.S. 6,569,696 B2) in view of Anai et al. (U.S. 6,458,208 B1) and Shimane (U.S. 2003/0017256 A1).

Suenaga et al. (Figs.3 and 4) teach a method to apply a resist in a surface of a substrate in a processing apparatus, wherein said processing apparatus includes a plurality of stacked units, wherein said stacked units includes a heating unit and a cooling unit, and wherein the process to apply the resist on the surface of the semiconductor substrate includes the steps pretreat the surface of the surface including thermally processing the surface of the substrate; and applying a resist onto the substrate after perform said pretreatment, wherein the step of thermally processing the substrate is performed in dehumidified air (column 4, line 26 – column 5, line 43).

Suenaga et al. fail to teach performing said thermal processing step for evaporating water form the surface of the substrate; and making the surface of the substrate hydrophobic with a hydrophobic processing material, wherein said hydrophobic processing material is hexamethyldisilazane. However, Anai et al. (Figs.3, 4, 10 and 11) teach a method of applying a resist material on a surface of a substrate in

a processing apparatus, wherein said processing apparatus includes a plurality of stacked units including a series of cleaning units (16, 18), a heating unit (17) and a cooling unit (19), and wherein said process includes the steps pretreat the surface of the surface including thermally processing for evaporating water from the surface of a substrate after performing a cleaning step, and making the surface of the substrate hydrophobic with hexamethyldisilazane vapor; and applying a resist onto the substrate after performing said pretreatment step (column 6, lines 4 – 50, and column 10, lines 4 – 36).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Suenaga et al. and Anai et al. to enable the pretreatment step of Suenaga et al. to be performed according to the teachings of Anai et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed pretreatment step of Suenaga et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07) and because this would result in a clean, hydrophobic semiconductor substrate (Anai et al., column 10, lines 4 – 35).

Suenaga et al. in combination with Anai et al. substantially teach all aspects of the invention but fail to disclose wherein a humidity of the dehumidified atmosphere is below 20% including 20%. However, Shimane in a related and conventional method to form photoresist layers teaches that applying conditions to required to form resist layers include temperature of the resist and ambient humidity and that such parameters are preset in order to obtain optimum conditions ([0006]). Therefore, it would be obvious to

one of ordinary skill in the art at the time the invention was made to combine the teachings of Suenaga et al. and Anai et al. with the teachings of Shimane et al. to enable independently controlling the temperature and humidity conditions of the resist deposition unit of Suenaga et al. and Anai et al. as taught by the conventional teachings of Shimane.

Still, the combined teachings of Suenaga et al., Anai et al. and Shimane fail to expressly teach wherein the step of thermal processing to the step of making the substrate surface hydrophobic is performed in a dehumidified atmosphere. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the atmosphere through the above-mentioned steps has to be dehumidified because the objective during said above mentioned steps as disclosed by the prior art of record is to keep the surface of the substrate dry and eventually hydrophobic.

3. Claim 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suenaga et al. (U.S. 6,569,696 B2) in view of Anai et al. (U.S. 6,458,208 B1).

Suenaga et al. (Figs.3 and 4) teach a method to apply a resist in a surface of a substrate in a processing apparatus, wherein said processing apparatus includes a plurality of stacked units, wherein said stacked units includes a heating unit and a cooling unit, and wherein the process to apply the resist on the surface of the semiconductor substrate includes the steps pretreat the surface of the surface including thermally processing the surface of the substrate; and applying a resist onto the substrate after perform said pretreatment, wherein the step of thermally processing the substrate is performed in dehumidified air (column 4, line 26 – column 5, line 43).

Suenaga et al. fail to teach performing said thermal processing step for evaporating water from the surface of the substrate; and making the surface of the substrate hydrophobic with a hydrophobic processing material, wherein said hydrophobic processing material is hexamethyldisilazane. However, Anai et al. (Figs. 3, 4, 10 and 11) teach a method of applying a resist material on a surface of a substrate in a processing apparatus, wherein said processing apparatus includes a plurality of stacked units including a series of cleaning units (16, 18), a heating unit (17) and a cooling unit (19), and wherein said process includes the steps pretreat the surface of the surface including thermally processing for evaporating water from the surface of a substrate after performing a cleaning step, and making the surface of the substrate hydrophobic with hexamethyldisilazane vapor; and applying a resist onto the substrate after performing said pretreatment step (column 6, lines 4 – 50, and column 10, lines 4 – 36).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Suenaga et al. and Anai et al. to enable the pretreatment step of Suenaga et al. to be performed according to the teachings of Anai et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed pretreatment step of Suenaga et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07) and because this would result in a clean, hydrophobic semiconductor substrate (Anai et al., column 10, lines 4 – 35).

The combined teachings of Suenaga et al. and Anai et al. fail to teach wherein in the step of thermally processing, a temperature of the substrate is above 150°C including 150°C. However, the pretreatment heating process disclosed in the combination of Suenaga et al. and Anai et al. is for the purpose to eliminate humidity from the surface of the substrate (Anai et al. column 6, lines 4 – 28). However, the selection of the temperature ranges in Suenaga et al. and Anai et al. are obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain desired deposition conditions. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to use the process of Suenaga et al. and Anai et al. to arrive at the claimed invention.

Response to Arguments

4. Applicant's arguments with respect to claims 1-17 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329.

Updates can be found at <http://www.uspto.gov/web/info/2800.htm>.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
December 6, 2004


George Fourson
Primary Examiner